C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142
100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF

P21 DNP ANALOG ADC0_6 ADC0_2 ADC0_5 ADC0_0

P20 DNP GPIO GPIO3_8 GPIO3_10 GPIO3_12 GPIO3_14 GPIO3_9 GPIO3_11 GPIO3_13 GPIO3_15

P19 DNP SPIFI
traces may be cut to install header and jumpers

R48 10k RESET
R49 10k
P5

U20 W25Q80BV
CS VCC DO HOLD WP CLK GND DI
C144 100nF

SPIFI_CS SPIFI_MOSI SPIFI_MISO SPIFI_SIO2 SPIFI_SIO3 SPIFI_SCK

U23
LPC43XXFBD144

ADC0_5/ADC1_5 ADC0_2/ADC1_2 ADC0_6/ADC1_6 VDDIO P7_7 ADC0_3/ADC1_3 ADC0_4/ADC1_4 VDDA ADC0_7/ADC1_7 VSSA P7_6 P7_5 P7_4 VDDREG WAKEUP0 RTC_ALARM RESET VBAT RTCX2 RTCX1 P3_8 P3_7 P3_6 P3_5 PE_4 P3_4 P3_3 P7_3 P5_2 P7_2 P3_1 P7_1 P3_0 VDDIO P7_0 VSSIO

GPIO3_8 GPIO3_10 GPIO3_12 GPIO3_14 GPIO3_9 GPIO3_11 GPIO3_13 GPIO3_15 GPIO3_11 I2S0_TX_SDA GPIO3_10 I2S0_TX_WS GPIO0_4 I2S0_TX_SCK VDDIO GPIO3_8

P4_0 ADC0_1/ADC1_1
RSSI P4_1
LED1 VSSIO
VDDIO
ADC0_0 ADC0_0/ADC1_0/DAC
SGPIO9 P4_3
LED2 P4_2
TXENABLE P4_4
RXENABLE P4_5
XCVR_EN P4_6
XTAL1 XTAL2
GP_CLKIN P4_7
SGPIO13 P4_8
USB0_VDDA3V3_DRIVER
USB0_VDDA3V3
DP USB0_DP
USB0_VSSA_TERM
DM USB0_DM
USB0_VBUS
USB0_ID
USB0_VSSA_REF
RREF USB0_RREF
TDI VDDREG
TCK TCK/SWDCLK
DBGEN DBGEN
TRST
TMS TMS/SWDIO
TDO TDO/SWO
SGPIO0 P0_0
SGPIO14 P4_9
SGPIO1 P0_1
SGPIO15 P4_10
VDDIO

P2_13 P7
VDDIO P9
P2_12
P2_11
P2_10 P10
P6_12 LED3
P2_9 P2_9
P6_11 VREGMODE
P6_10 EN1V8
CLK2 I2S0_TX_MCLK
P2_8 P2_8
P6_9 ISP
P2_7
P2_6 MIXER_SCLK
VDDREG
I2C0_SDA SDA
I2C0_SCL SCL
P2_5 P11
USB1_DM
USB1_DP
P2_4 P12
P2_3 P13
P6_8 USB0_IND0
P6_7 USB0_IND1
P2_2 SGPIO6
P6_6 SGPIO5
P6_5 CPLD_TDI
P2_1 U0_RXD
P6_4 MIXER_SDATA
P6_3 SGPIO4
P6_2 CPLD_TMS
VDDIO
VSSIO U0_TXD
P2_0 CPLD_TCK
P6_1
P6_0

P5_0 P1_0 P5_1 VSSIO VDDIO P1_1 P1_2 P1_3 CLKO P5_2 P1_4 P1_5 P1_6 P1_7 P1_8 P1_9 P1_10 P5_3 P1_11 P1_12 P5_4 P5_5 VDDREG P1_13 P1_14 P1_15 P5_6 P1_16 P5_7 P1_17 P1_18 P1_19 P9_5 P1_20 VDDIO P9_6

RF_1DQ_ENABLE SGPIO7 SD_CLK SSP1_MISO SSP1_MOSI SD_POW SD_CMD SD_VOLT0 SD_DAT0 SD_DAT1 SD_DAT2 SD_DAT3 MIXER_ENRX MIXER_RESETX SD_CD SGPIO10 SGPIO2 SGPIO3 CS_AD SGPIO11 SGPIO12 SSP1_SCK CPLD_TDO CS_XCVR SGPIO8 SGPIO_CLK

P22 DNP I25
I2S0_TX_WS I2S0_TX_MCLK I2S0_TX_SDA I2S0_TX_SCK

P25 LPC_ISP DNP
RESET U0_TXD U0_RXD ISP

R46 1% 162k
R47 1% 330k
33pF C125
C126 C127 10uF 10uF
L10 4u7
REG_OUT2
P1 1V8 DNP

R50 DNP
R51 10k VREGMODE
R53 DNP

U21 TPS62410
ADJ2 MODE/DATA VIN FB1 DEF1 SW2 EN2 GND EN1 SW1 PP
VBUS
EN1V8
R52 10k VBUS
R54 10k
C143 10uF
C145 C146 10uF 10uF
L11 4u7

R55 1% 162k
R56 1% 15k
REG_OUT1
P8 VCC DNP
P3 GND DNP

bank 1 power selection
R60 DNP
R64 0 DNP
VCCIO1

C148 C149 C150 C151 C152 C153 C154
100nF 100nF 100nF 100nF 100nF 100nF 100nF

U22 GSG-IP4220CZ6
ESD1 ESD4 GND VP ESD2 ESD3
GSG-USB-MICRO-B
GND ID D+ D- VBUS J1
R57 0
R58 0
FB1 FILTER
C147 100nF
R62 0
R65 10k DNP

P26 DNP LPC_JTAG
Cortex Debug Connector (10 pin 50 mil)
RESET
R63 10k
R64 10k
R66 10k
P23
P24 TMS
TDI
TCK
DBGEN
TRST
TMS
TDO
R69 1% 12k RREF

P28 SD
SD_CD SD_DAT2 SD_DAT0 SD_CMD SD_CLK SD_DAT3 SD_DAT1 SD_VOLT0 SD_POW
DNP

LED1 LED2 LED3 VCCLED EN1V8
R72 470
R73 470
R74 470
R75 470
R76 470
D4 D5 D6 D7 D8

Boot selection:

	P2_9	P2_8	P1_2	P1_1
USART0	GND	GND	GND	GND
SPIFI	GND	GND	GND	VCC
USB0	GND	VCC	GND	VCC
SSP0	GND	VCC	VCC	VCC
USART3	VCC	GND	GND	GND

P1_1 R67 10k 10k DNP R40 P27 CONN_3
P2_8 R82 10k 10k DNP R7 P32 CONN_3
P1_2 R42 DNP 10k 10k DNP R68 P33 CONN_3
P2_9 R43 DNP 10k 10k DNP R93 P34 CONN_3
Default boot configuration is SPIFI. Install headers and jumpers (and optionally resistors) to reconfigure.

U23 starts up on this 12 MHz crystal. This makes it possible to use USB0 DFU boot mode. It should be possible to switch to GP_CLKIN provided by the clock generator IC (MCU_CLK) if desired.
X2 MCU_XTAL
C157 18pF
C158 18pF
MCU_CLK C155 100pF GP_CLKIN C156 47pF
C155 and C156 values are a guess. The datasheet doesn't state the acceptable voltage range for GP_CLKIN.

P30 BANK2_AUX DNP
B2AUX1 B2AUX3 B2AUX5 B2AUX7 B2AUX9 B2AUX11 B2AUX13 B2AUX15 B2AUX2 B2AUX4 B2AUX6 B2AUX8 B2AUX10 B2AUX12 B2AUX14 B2AUX16
P31 BANK1_AUX DNP
B1AUX9 B1AUX11 B1AUX13 B1AUX15 B1AUX10 B1AUX12 B1AUX14 B1AUX16

Series resistors are here because of a possible overshoot/undershoot problem. They may be able to be removed safely. Anyway, they probably will minimize damage in the event of SGPIO/CPLD misconfiguration.

R77 39 SGPIO9 BANK2F3M1
R78 39 SGPIO13 BANK2F3M2
R79 39 SGPIO0 BANK2F3M3
R80 39 SGPIO14 BANK2F3M4
R81 39 SGPIO1 BANK2F3M5
R86 39 SGPIO15 BANK2F3M6
R87 39 SGPIO7 BANK2F3M7
R88 39 SGPIO10 BANK2F3M8
R89 39 SGPIO2 BANK2F3M9
R90 39 SGPIO3 BANK2F3M10
R91 39 SGPIO11 BANK2F3M11
R96 39 SGPIO12 BANK2F3M12
R97 DNP 39 SGPIO8 BANK2F3M13
R98 39 SGPIO4 BANK2F3M14
R99 39 SGPIO5 BANK2F3M15
R100 39 SGPIO6 BANK2F3M16

U24 GSG-XC2C64A-7VQG100C
B2AUX12 B2AUX11 B2AUX10 B2AUX9 B2AUX8 B2AUX7 B2AUX6 B2AUX5 B2AUX4 B2AUX3 B2AUX2 B2AUX1
DD9 DD8 DD7
P35 GCK1 DD6
BANK2F1M12 BANK2F1M11 BANK2F1M10 VAUX BANK2F1M9 BANK2F1M8 BANK2F1M7 BANK2F1M6 BANK2F1M5 BANK2F1M4 BANK2F1M3 BANK2F1M2 BANK2F1M1 BANK1F2M1 BANK1F2M2 BANK1F2M3 BANK1F2M4 BANK1F2M5 BANK1F2M6 BANK1F2M7 BANK1F2M8 BANK1F2M9
BANK2F3M9 BANK2F3M10 BANK2F3M11 BANK2F3M12 BANK2F3M13 BANK2F3M14 BANK2F3M15 BANK2F3M16 B1AUX16 B1AUX15 B1AUX14 B1AUX13 B1AUX12 B1AUX11 VCCIO1
BANK1F2M10 BANK1F2M11 BANK1F2M12 BANK1F2M13 BANK1F2M14 BANK1F2M15 BANK1F2M16 BANK1F4M1 BANK1F4M2 BANK1F4M3 BANK1F4M4 BANK1F4M5 BANK1F4M6 BANK1F4M7 BANK1F4M8 BANK1F4M9 BANK1F4M10
CPLD_TDI CPLD_TMS CPLD_TCK B1AUX9 B1AUX10

P29 CPLD_JTAG DNP
CPLD_TMS CPLD_TDI CPLD_TDO CPLD_TCK

R97 may be installed to connect SGPIO8 to the CPLD. By default SGPIO8 is used as a clock input.

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File: mcu.sch
Sheet: /mcu/usb/power/
Title: Jawbreaker
Size: User | Date: 6 nov 2012 | **Rev:**
KiCad E.D.A. eeschema (2012-05-21 BZR 3261)-stable | Id: 4/4

C84 C85 C86 C87 C89 C90 C91 C92 C93 C94
22pF 22pF 22pF 10nF 10nF 100pF 100nF 10nF 10nF 22pF

C88
10nF

C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83
100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF

SSP1_SCK SCLK_XCVR
SSP1_MOSI DIN_XCVR
SSP1_MISO DOUT_XCVR
R41 39
R42 39
DIN_AD
SCLK_AD
Install R18 and R19 only if 1V8 is used for U18.
DNP R18 47
R19 47 DNP

DNP L13 INDUCTOR
1uF C159 DNP
RF_LDO_ENABLE
DNP U26 RF LDO
VIN VOUT GND NC EN
DNP L14 INDUCTOR
C117 DNP
remove FB2 if optional RF LDO is installed
FILTER FB2
C105 10uF
P36 VAA DNP

serial test points
P37 SCL
P38 SDA
P39 SSP1_SCK
P40 SSP1_MOSI
P41 SSP1_MISO

RX_IF
RX_BALUN T3
L6 DNP
C99 22pF
L7 6.2nH
C102 22pF
TX_IF
TX_BALUN T4
L8 DNP
C104 3pF
L9 DNP
C111 3pF

U17 MAX2837
EP
VCCRXLNA GNDRXLNA B5 RXRF+ RXRF− B4 VCCTXPAD B3 B2 TXRF+ TXRF− B1
RXENABLE TXENABLE VCCRXMX TXBBQ− TXBBQ+ TXBBI+ TXBBI− VCCRXFL RXHP VCCRXVGA RXBBI+ RXBBI−
RXBBQ+ RXBBQ− B6 B7 RSSI DIN CS DOUT VCCVCO BYPASS GNDVCO ENABLE
VCCTXMX PABIAS SCLK CLOCKOUT XTAL2 XTAL1 VCCXTAL VCCDIG VCCCP GNDCP CPOUT+ CPOUT−
SCLK_XCVR XCVR_CLKOUT XTAL2
RSSI DIN_XCVR CS_XCVR DOUT_XCVR XCVR_EN
R41 4k7
C106 1uF

TXBBQ− TXBBQ+ TXBBI+ TXBBI− RXBBI+ RXBBI−
C95 DNP 22pF
C96 DNP 22pF
R14 4k7 R15 4k7 R16 4k7 R17 4k7
1k R8 1k R9 1k R10 1k R13
QD+ QD− ID− ID+
R20 0 R21 0 R22 0 R23 0
C101 DNP 22pF
C103 DNP 22pF
C107 DNP 22pF C108 DNP 22pF C109 DNP 22pF C110 DNP 22pF

C97 330nF COM
C98 330nF REFN
C100 330nF

U18 MAX5864
EP
REFN COM REFIN ID+ ID− VDD GND QD− QD+ VDD NC GND
REFP VDD IA+ IA− GND CLK GND VDD QA− QA+ VDD GND
CLK0
CS SCLK DIN VDD DD9 DD8 DD7 DD6 DD5 DD4 DD3 DD2
DA0 DA1 DA2 DA3 OGND OVDD DA4 DA5 DA6 DA7 DD0 DD1

C112 180pF
C114 3.3nF
R25 475
R26 475

X1 GSG-XTAL4PIN
C113 100nF
C115 10nF
C116 DNP
R27 1k8 R28 1k8 R104 4k7
U19 SI5351C
GND VDD XA XB INTR SCL SDA CLKIN OEB CLK3 CLK2 VDDOB CLK4 VDDOC CLK5 CLK6 CLK7 VDDOD CLK0 CLK1 VDDOA
MIX_CLK MCU_CLK GCK1 GCK2 SGPIO_CLK
P15 INTR SCL SDA P14 P18

CLK0 is at the sample rate
CLK1 is at sample rate x2
CLK2 is at sample rate x2

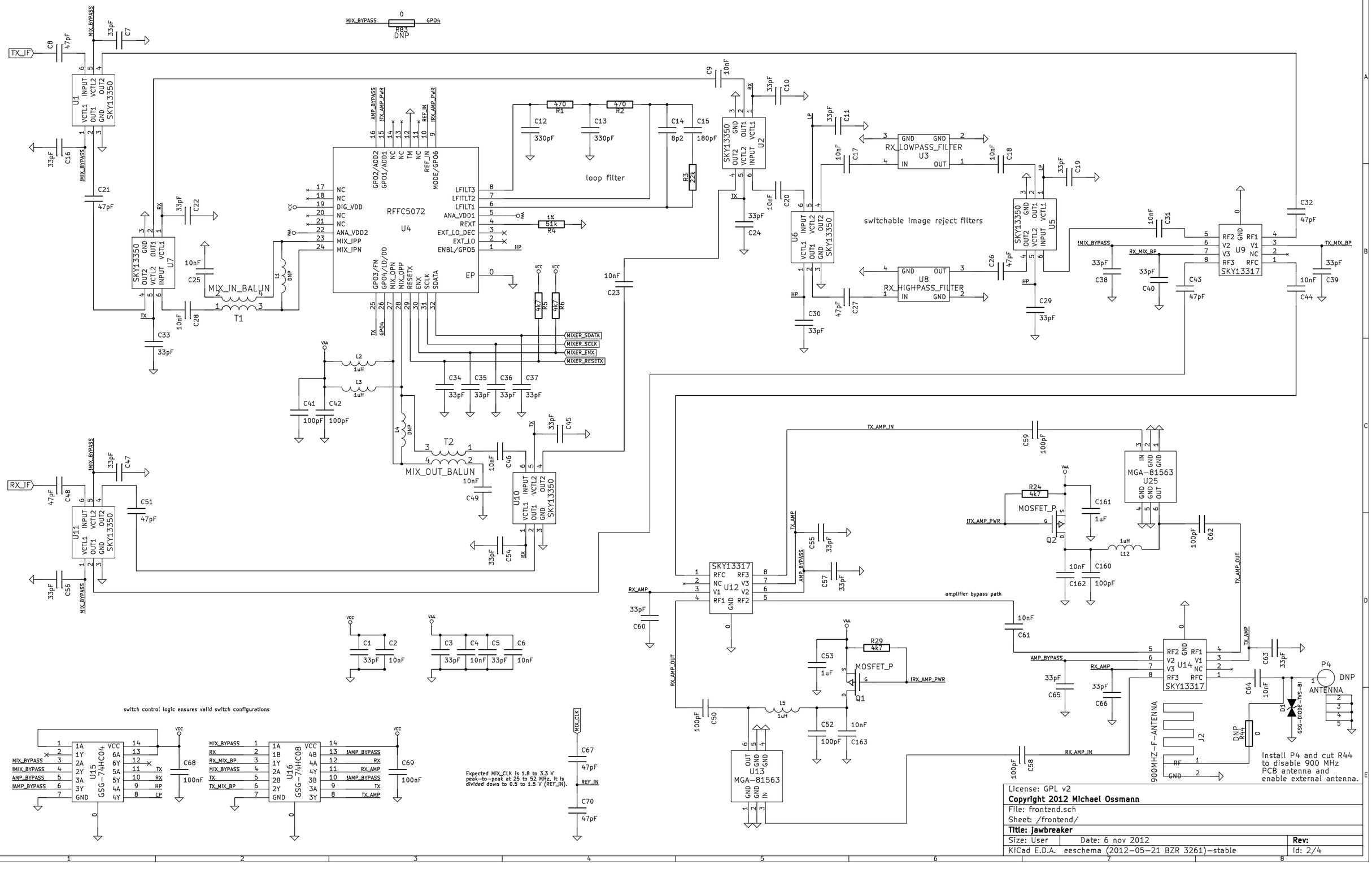
P16 CLKIN
C118 DNP C164 DNP
R45 DNP R84 50 DNP R85 DNP
CLKIN_JMP P17 DNP
Cut P17 short and install P16 and P17 to enable external clock input. If short is cut, a jumper should be used on P17 at all times when an external clock is not connected to P16.
Install C118, C164, R45, R84, and R85 as necessary to match input.
For CMOS input, install 0 ohm resistors in place of C118 and C164; do not install R45, R84, or R85.

Install C165, and R92 as necessary to match output.
For CMOS output, install 0 ohm resistor in place of C165; do not install R92.
C165 DNP
P2 CLKOUT DNP
R92 50 DNP
4k7 R105

Use 0 ohm resistors to select clock output voltage.
1V8 VCC
DNP R30 0 R31 DNP
DNP R32 0 R33 DNP
DNP R34 0 R35 DNP
DNP R36 0 R37 DNP
VDDOA VDDOB VDDOC VDDOD
C119 100nF C120 100nF C121 100nF C122 100nF

Use 0 ohm resistors to select MAX5864 I/O voltage.
DNP R38 0 R39 DNP
OVDD
C123 100nF C124 2.2uF

File: baseband.sch
Sheet: /baseband/
Title: jawbreaker
Size: User | Date: 6 nov 2012 | **Rev:**
KiCad E.D.A. eeschema (2012-05-21 BZR 3261)-stable | Id: 3/4



File: frontend.sch
Sheet: /frontend/

Title: jawbreaker

Size: User	Date: 6 nov 2012	**Rev:**
KiCad E.D.A. eeschema (2012-05-21 BZR 3261)-stable		Id: 2/4