C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142
100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF

P21 ANALOG DNP — ADC0_6 ADC0_2 ADC0_5 ADC0_0

P20 GPIO DNP — GPIO3_8 GPIO3_10 GPIO3_12 GPIO3_14 GPIO3_9 GPIO3_11 GPIO3_13 GPIO3_15

P19 SPIFI DNP — traces may be cut to install header and jumpers

R48 10k R49 10k P5 RBSBT

U20 W25Q80BV — CS DO WP GND VCC HOLD CLK DI — C144 100nF

SPIFI_CS SPIFI_MOSI SPIFI_MISO SPIFI_SIO2 SPIFI_SIO3 SPIFI_SCK P6

U22 GSG-IP4220CZ6 — BSD1 BSD4 GND VP BSD2 BSD3

GSG-USB-MICRO-B J1 — GND ID D+ D- VBUS

R57 0 R58 0 FB1 FILTBR VBUS C147 100nF R62 0

R65 10k DNP

U23 LPC43XXFBD144

1	P4_0		
2	ADC0_1/ADC1_1	RSSI	
3	P4_1	LBD1	
4	VSSIO		
5	VDDIO		
6	ADC0_0/ADC1_0/DAC	ADC0_0	
7	P4_3	SGPIO9	
8	P4_2	LBD2	
9	P4_4	TXBNABLB	
10	P4_5	RXBNABLB	
11	P4_6	XCVR_BN	
12	XTAL1	XTAL1	
13	XTAL2	XTAL2	
14	P4_7	GP_CLKIN	
15	P4_8	SGPIO13	
16	USB0_VDDA3V3_DRIVER		
17	USB0_VDDA3V3		
18	USB0_DP	DP	
19	USB0_VSSA_TERM		
20	USB0_DM	DM	
21	USB0_VBUS		
22	USB0_ID		
23	USB0_VSSA_RBF		
24	USB0_RREF	RREF	
25	VDDREG		
26	TDI	TDI	
27	TCK/SWDCLK	TCK	
28	DBGEN	DBGEN	
29	TRST	P24	
30	TMS/SWDIO	TMS	
31	TDO/SWO	TDO	
32	P0_0	SGPIO0	
33	P4_9	SGPIO14	
34	P0_1	SGPIO1	
35	P4_10	SGPIO15	
36	VDDIO		
37	P5_0	RF_LDO_ENABLE	
38	P1_0	SGPIO7	
39	P5_1		
40	VSSIO		
41	VDDIO		
42	P1_1		
43	P1_2		
44	P1_3		
45	CLKO		
46	P5_2		
47	P1_4	SSP1_MISO	
48	P1_5	SD_CLK	
49	P1_6	SSP1_MOSI	
50	P1_7	SD_POW	
51	P1_8	SD_CMD	
52	P1_9	SD_VOLT0	
53	P1_10	SD_DAT0	
54	P5_3	SD_DAT1	
55	P1_11	SD_DAT2	
56	P1_12	SD_DAT3	
57	P5_4		
58	P5_5	MIXER_ENX	
59	VDDREG	MIXER_RESETX	
60	P1_13	SD_CD	
61	P1_14	SGPIO10	
62	P1_15	SGPIO2	
63	P5_6		
64	P1_16	SGPIO3	
65	P5_7	CS_AD	
66	P1_17	SGPIO11	
67	P1_18	SGPIO12	
68	P1_19	SSP1_SCK	
69	P9_5	CPLD_TDO	
70	P1_20	CS_XCVR	
71	VDDIO		
72	P9_6	SGPIO_CLK	
73	P6_0		
74	CPLD_TCK		
75	U0_TXD		
76	VSSIO		
77	VDDIO		
78	CPLD_TMS		
79	SGPIO4		
80	MIXBR_SDATA		
81	U0_RXD		
82	CPLD_TDI		
83	SGPIO5		
84	SGPIO6		
85	USB0_IND1		
86	USB0_IND0		
87	P13		
88	P12		
89			
90			
91	P11		
92	I2C0_SCL	SCL	
93	I2C0_SDA	SDA	
94	VDDRBG		
95	P2_6	MIXBR_SCLK	
96	P2_7		
97	P2_8		
98	CLK2	P2_8	
99	P6_10	I2S0_TX_MCLK	
100	P6_11	BN1V8	
101	P6_9	VRBGMODB	
102	P2_9	P2_9	
103	P6_12	LBD3	
104	P2_10	P10	
105	P2_11		
106	P2_12	P9	
107	VDDIO	P7	
108	P2_13		

R59 10k ISP

P22 I2S — I2S0_TX_WS I2S0_MCLK I2S0_TX_SDA I2S0_TX_SCK — DNP

P25 LPC_ISP DNP — RBSBT U0_TXD U0_RXD ISP

bank 1 power selection: R60 0 DNP, R61 0 DNP — VCC 1V8 VCCIO1

C148 C149 C150 C151 C152 C153 C154 100nF

P26 LPC_JTAG DNP — Cortex Debug Connector (10 pin 50 mil) — RESET P23 P24

R63 10k R64 10k R66 10k

R67 10k DNP P1_1 — R82 10k DNP P2_8 — R40 10k R7 10k — P27 P32 CONN_3

R42 10k DNP P1_2 — R43 10k DNP P2_9 — R68 10k R93 10k — P33 P34 CONN_3

Default boot configuration is SPIFI. Install headers and jumpers (and optionally resistors) to reconfigure.

Boot selection:

	P2_9	P2_8	P1_2	P1_1
USART0	GND	GND	GND	GND
SPIFI	GND	GND	GND	VCC
USB0	GND	VCC	GND	VCC
SSP0	GND	VCC	VCC	VCC
USART3	VCC	GND	GND	GND

LED1 LED2 LED3 VCCLED ENV1V8 — R72 470 R73 470 R74 470 R75 470 R76 470 — D4 D5 D6 D7 D8

P28 SD DNP — SD_CD SD_DAT2 SD_DAT0 SD_CMD SD_CLK SD_DAT3 SD_DAT1 SD_VOLT0 SD_POW

U23 starts up on this 12 MHz crystal. This makes it possible to use USB0 DFU boot mode. It should be possible to switch to GP_CLKIN provided by the clock generator IC (MCU_CLK) if desired.

X2 MCU_XTAL — XTAL1 XTAL2 — C157 18pF C158 18pF

MCU_CLK C155 100pF GP_CLKIN C156 47pF

C155 and C156 values are a guess. The datasheet doesn't state the acceptable voltage range for GP_CLKIN.

P30 BANK2_AUX DNP — B2AUX1 B2AUX3 B2AUX5 B2AUX7 B2AUX9 B2AUX11 B2AUX13 B2AUX15 — B2AUX2 B2AUX4 B2AUX6 B2AUX8 B2AUX10 B2AUX12 B2AUX14 B2AUX16

P31 BANK1_AUX DNP — B1AUX9 B1AUX11 B1AUX13 B1AUX15 — B1AUX10 B1AUX12 B1AUX14 B1AUX16

Series resistors are here because of a possible overshoot/undershoot problem. They may be able to be removed safely. Anyway, they probably will minimize damage in the event of SGPIO/CPLD misconfiguration.

SGPIO9	R77 39	BANK2F3M1	
SGPIO13	R78 39	BANK2F3M2	
SGPIO0	R79 39	BANK2F3M3	
SGPIO14	R80 39	BANK2F3M4	
SGPIO1	R81 39	BANK2F3M5	
SGPIO15	R86 39	BANK2F3M6	
SGPIO7	R87 39	BANK2F3M7	
SGPIO10	R88 39	BANK2F3M8	
SGPIO2	R89 39	BANK2F3M9	
SGPIO3	R90 39	BANK2F3M10	
SGPIO11	R91 39	BANK2F3M11	
SGPIO12	R96 39	BANK2F3M12	
SGPIO8 DNP	R97 39	BANK2F3M13	
SGPIO4	R98 39	BANK2F3M14	
SGPIO5	R99 39	BANK2F3M15	
SGPIO6	R100 39	BANK2F3M16	

R97 may be installed to connect SGPIO8 to the CPLD. By default SGPIO8 is used as a clock input.

P29 CPLD_JTAG DNP — CPLD_TMS CPLD_TDI CPLD_TDO CPLD_TCK

R46 162k 1% — R47 330k 1% — C125 33pF — L10 4u7 — C126 10uF C127 10uF — P1 1V8 DNP — RBG_OUT2

VRBGMODB R51 10k — R50 DNP R53 DNP

U21 TPS62410 — ADJ2 MODB/DATA VIN FB1 DBF1 PP — SW2 BN2 GND BN1 SW1 — VBUS C143 10uF — R52 10k VBUS — R54 10k BN1V8 — L11 4u7 — C145 C146 10uF

R55 162k 1% — R56 715k 1% — RBG_OUT1 — P3 GND DNP — P8 VCC DNP

U24 GSG-XC2C64A-7VQG100C

B2AUX12	1	BANK2F1M12		NC	75
B2AUX11	2	BANK2F1M11		BANK2F3M9	74
B2AUX10	3	BANK2F1M10		NC	73
B2AUX9	4	BANK2F1M9		BANK2F3M10	72
	5	VAUX		BANK2F3M11	71
B2AUX8	6	BANK2F1M8		BANK2F3M12	70
B2AUX7	7	BANK2F1M7		GND	69
B2AUX6	8	BANK2F1M6		BANK2F3M13	68
B2AUX5	9	BANK2F1M5		BANK2F3M14	67
B2AUX4	10	BANK2F1M4		NC	66
B2AUX3	11	BANK2F1M3		NC	65
B2AUX2	12	BANK2F1M2		BANK2F3M15	64
B2AUX1	13	BANK2F1M1		NC	63
	14	BANK1F2M1		GND	62
	15	BANK1F2M2		BANK2F3M16	61
	16	BANK1F2M3		BANK1F4M16	60
DD9	17	BANK1F2M4		NC	59
DD8	18	BANK1F2M5		BANK1F4M15	58
DD7	19	BANK1F2M6		VCC	57
	20	NC		BANK1F4M14	56
	21	GND		BANK1F4M13	55
P35	22	BANK1F2M7		NC	54
GCK1	23	BANK1F2M8		BANK1F4M12	53
DD6	24	BANK1F2M9		BANK1F4M11	52
	25	NC		VCCIO1	51

| | | | | |

C84 C85 C86 C87 C89 C90 C91 C92 C93 C94
22pF 22pF 22pF 10nF 10nF 100pF 100nF 10nF 10nF 22pF

C88
10nF

C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C82 C83
100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF 2.2uF 100nF

SSP1_SCK SCLK_XCVR
SSP1_MOSI DIN_XCVR
SSP1_MISO DOUT_XCVR
R41 39
R42 39
DIN_AD
SCLK_AD
Install R18 and R19 only if 1V8 is used for U18.
DNP R18 47
DNP R19 47

DNP L13 INDUCTOR
1uF C159
RF_LDO_BNABLB
DNP U26 RF LDO VIN VOUT GND BN NC
DNP C117
remove FB2 if optional RF LDO is installed
DNP L14 INDUCTOR
FILTER FB2
C105 10uF
P36 DNP

TXBBQ− TXBBQ+ TXBBI+ TXBBI−
DNP C95 22pF
DNP C96 22pF
1k R8 1k R9 1k R10 1k R13
QD+ QD− ID− ID+
4k7 R14 4k7 R15 4k7 R16 4k7 R17
RXENABLE TXENABLE VCCRXMX TXBBQ− TXBBQ+ TXBBI+ TXBBI− VCCRXFL RXIP VCCRXVGA RXBBI+ RXBBI−
RXBBI+ RXBBI−

C100 330nF
330nF C97 330nF C98
COM RBFN
REFP COM REFN ID+ ID− VDD GND QD− QD+ VDD NC GND

RX_IF
RX_BALUN T3
DNP 22pF C99
DNP L6
L7 6.2nH
22pF C102
TX_IF
TX_BALUN T4
3pF C104
DNP L8
DNP L9
3pF C111

U17 MAX2837
BP VCCRXLNA GNDRXLNA B5 RXRF+ RXRF− B4 VCCTXPAD B3 B2 TXRF+ TXRF− B1
RXBBQ+ RXBBQ− B6 B7 RSSI DIN CS DOUT VCCVCO BYPASS GNDVCO BNABLB
RSSI DIN_XCVR CS_XCVR DOUT_XCVR XCVR_BN
VCCTXMX PABIAS SCLK CLOCKOUT XTAL2 XTAL1 VCCXTAL VCCDIG VCCCP GNDCP CPOUT+ CPOUT−
SCLK_XCVR XCVR_CLKOUT XTAL2 P14
CPOUT+ CPOUT−
475 R25 180pF C112 475 R26
3.3nF C114
R41 4k7
C106 1uF

0 R20 0 R21 0 R22 0 R23
DNP C101 22pF
DNP C103 22pF
DNP C107 22pF DNP C108 22pF DNP C109 22pF DNP C110 22pF

U18 MAX5864
BP REFP VDD IA+ IA− GND CLK GND VDD QA− QA+ VDD GND
CLK0
QA− QA+
CS SCLK DIN VDD DD9 DD8 DD7 DD6 DD5 DD4 DD3 DD2
CS_AD SCLK_AD DIN_AD DD9 DD8 DD7 DD6 DD5 DD4 DD3 DD2
DA0 DA1 DA2 DA3 OGND OVDD DA4 DA5 DA6 DA7 DDD DD1
OVDD

serial test points
P37 SCL
P38 SDA
P39 SSP1_SCK
P40 SSP1_MOSI
P41 SSP1_MISO

C113 100nF
MIX_CLK
X1 GSG-XTAL4PIN
R27 118
R28 118
R104 47
P15 INTR SCL SDA
U19 SI5351C
GND XA XB INTR SCL SDA VDD VDDOC CLK4 CLK5 CLK6 CLK7 VDDOD CLK0 CLK1 VDDOA CLKIN OEB CLK3 CLK2 VDDOB
MCU_CLK VDDOD GCK1 GCK2 VDDOA
CLK0 is at the sample rate
CLK1 is at sample rate x2
CLK2 is at sample rate x2
C115 10nF
C116 100pF

P16 DNP CLKIN
DNP C118 DNP C164 DNP R45
DNP R84 50 DNP R85
DNP CLKIN_JMP P17
39 R94 SGPIO_CLK
4k7 R105
P18
Cut P17 short and install P16 and P17 to enable external clock input. If short is cut, a jumper should be used on P17 at all times when an external clock is not connected to P16.
Install C118, C164, R45, R84, and R85 as necessary to match input.
For CMOS input, install 0 ohm resistors in place of C118 and C164; do not install R45, R84, or R85.

DNP C165
DNP R92 50
P2 DNP CLKOUT
Install C165, and R92 as necessary to match output.
For CMOS output, install 0 ohm resistor in place of C165; do not install R92.

Use 0 ohm resistors to select clock output voltage.
1V8 VCC
DNP R30 0 R31 DNP VDDOA C119 100nF
DNP R32 0 R33 DNP VDDOB C120 100nF
DNP R34 0 R35 DNP VDDOC C121 100nF
DNP R36 0 R37 DNP VDDOD C122 100nF

Use 0 ohm resistors to select MAX5864 I/O voltage.
1V8 VCC
DNP R38 0 R39 DNP OVDD C123 100nF C124 2.2uF

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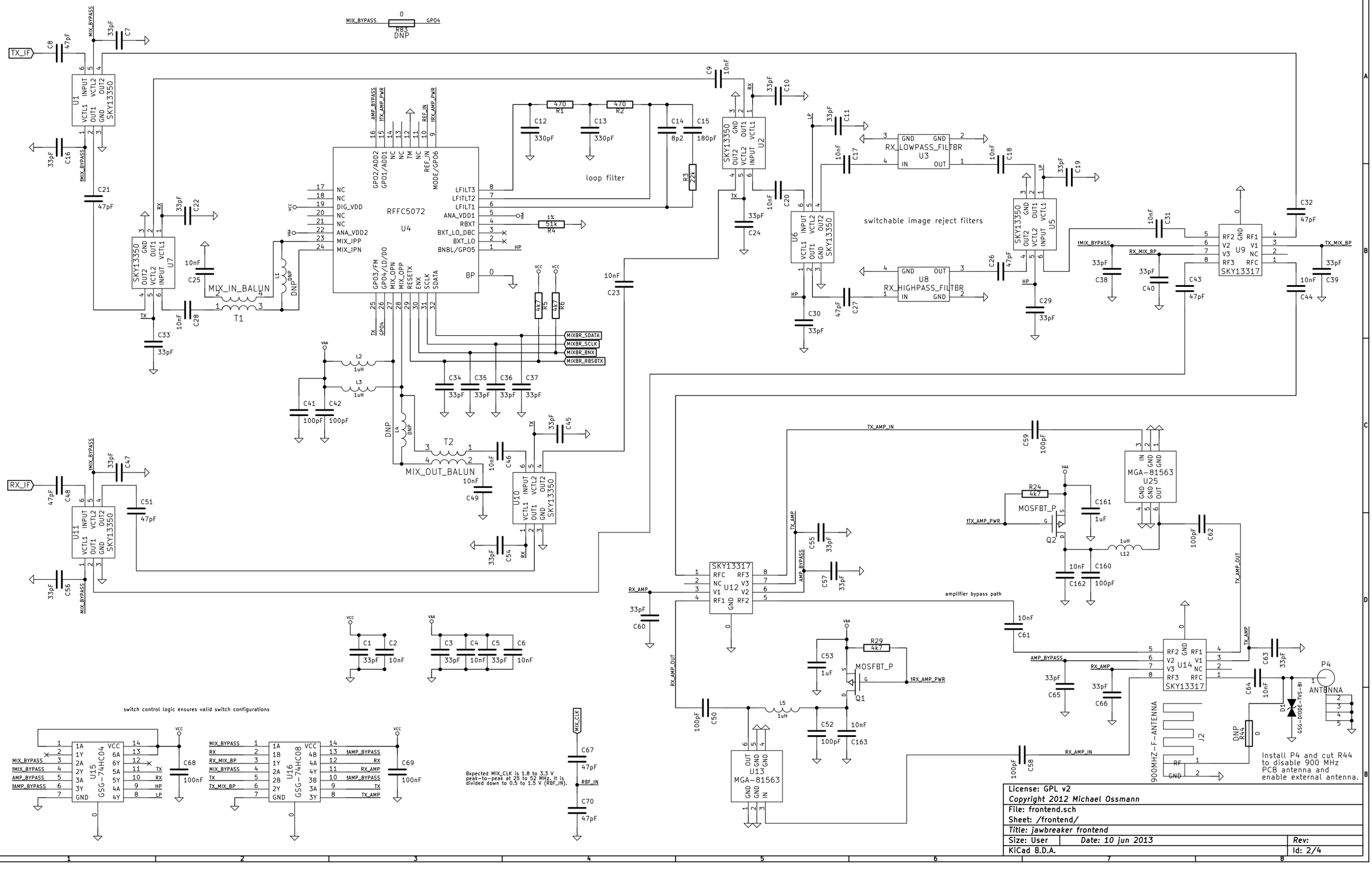

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