C128 C129 C130 C131 C132 C133 C134 C135 C137 C138 C139 C140 C141 C142
100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF

DNP
LPC_ISP
P25
RESET
U0_TXD
U0_RXD
ISP

RTC_XTAL
X3
RTCX1 RTCX2
C118 18pF
C164 18pF

R35 DNP
C155 DNP
DNP
USB_SHIELD
P80
SHIELD
DNP

U15
LXES1TBCC2-004
ESD1 NC
GND VDD
ESD2 NC

USB-MICRO-B
J1
GND
ID
D+
D-
VBUS
SHIELD

R12 10k
FB1
FILTER
C117 100nF
R62 0
P71

R48 10k
C136 100nF

U20
W25Q80BV
CS VCC
DO HOLD
WP CLK
GND DI
C144 100nF

U23
LPC4320FBD144

P4_0 HP
ADC0_1/ADC1_1 RSSI
P4_1 LED1
VSSIO
VDDIO
ADC0_0/ADC1_0/DAC ADC0_0
P4_3 SGPIO9
P4_2 LED2
P4_4 TXENABLE
P4_5 RXENABLE
P4_6 XCVR_EN
XTAL1
XTAL2
P4_7 GP_CLKIN
P4_8 SGPIO13
USB0_VDDA3V3_DRIVER
USB0_VDDA3V3
USB0_DP DP
USB0_VSSA_TERM
USB0_DM DM
USB0_VBUS
USB0_ID
USB0_VSSA_REF
USB0_RREF
VDDREG
TDI
TCK/SWDCLK
DBGEN
TRST
TMS/SWDIO
TDO/SWO
P0_0 SGPIO0
P4_9 SGPIO14
P0_1 SGPIO1
P4_10 SGPIO15
VDDIO

ADC0_5/ADC1_5 ADC0_2/ADC1_2 ADC0_6/ADC1_6 VDDIO P7_7 GPIO3_15
ADC0_3/ADC1_3 ADC0_4/ADC1_4 VDDA ADC0_7/ADC1_7 VSSA P7_6 P7_5 P7_4 VDDREG WAKEUP0 RTC_ALARM RESET VBAT RTCX2 RTCX1
P3_8 P3_7 P3_6 P3_5 PE_4 P3_3 P3_2 P7_2 P3_1 P7_1 P3_0 VDDIO P7_0 VSSIO
SPIFI_CS SPIFI_MOSI SPIFI_MISO SPIFI_SIO2 SPIFI_SIO3 SPIFI_SCK
GPIO3_11 I2S0_RX_SDA GPIO3_10 I2S0_RX_WS GPIO3_9 I2S0_TX_SCK GPIO3_8 I2S0_TX_WS

P2_13 P2_13
VDDIO
P2_12 IRX_AMP_PWR
P2_11 RX_AMP
P2_10 AMP_BYPASS
P6_12 LED3
P2_9 P2_9
P6_11 VREGMODE
P6_10 EN1V8
CLK2 I2S0_TX_MCLK
P2_8 P2_8
P6_9 ITX_AMP_PWR
P2_7
P2_6 MIXER_SCLK
VDDREG
I2C0_SDA SDA
I2C0_SCL SCL
P2_5 RX
USB1_DM
USB1_DP
P2_4 I2C1_SCL
P2_3 I2C1_SDA
P6_8 MIX_BYPASS
P6_7 TX
P2_2 SGPIO6
P6_6 SGPIO5
P6_5 CPLD_TMS
P2_1 U0_RXD
P6_4 MIXER_SDATA
P6_3 SGPIO4
P6_2 CPLD_TDI
VDDIO
VSSIO
P2_0 U0_TXD
P6_1 CPLD_TCK
P6_0 I2S0_RX_MCLK

R59 10k ISP

P69 VREGMODE
R51 10k VIN
C143 10uF
C147 100nF
U21
TPS62410
ADJ2 MODE/DATA
VIN FB1
DEF1 PP
SW2 EN2
GND EN1
SW1
REG_OUT1
REG_OUT2
R52 10k VIN
R54 10k
P70 EN1V8
L11 4u7
C145 10uF
C146 10uF
L10 4u7
C126 10uF
C127 10uF
P1 1V8 DNP
PCB trace jumper
R46 1% 162k
R47 1% 330k
C125 33pF
R55 1% 162k
R56 1% 715k
P8 VCC DNP
P3 GND DNP

See also I2S0 pins on P20.
P22
I2S
CLKOUT CLKIN
RESET
I2C1_SCL I2C1_SDA
SPIFI_MISO SPIFI_SCK
SPIFI_MOSI
I2S0_RX_SCK
I2S0_RX_SDA I2S0_RX_MCLK
I2S0_RX_WS I2S0_TX_SCK
I2S0_TX_MCLK
U0_RXD U0_TXD
P2_9 P2_13
P2_8 SDA
CLK6 SCL

C148 C149 C150 C153 C154 C151 C152
100nF 100nF 100nF 100nF 100nF 100nF 100nF

P20
GPIO
VBAT RTC_ALARM
WAKEUP
GPIO3_8 GPIO3_9 /I2S0_TX_WS
I2S0_TX_SDA/ GPIO3_10 GPIO3_11
GPIO3_12 GPIO3_13
GPIO3_14 GPIO3_15
ADC0_6
ADC0_2
ADC0_5
ADC0_0
VIN VBUS
PCB trace jumper

P26
LPC_JTAG
Cortex Debug Connector (10 pin 50 mil)
RESET
P23
TDI
TCK
DBGEN
TRST
TMS
TDO
R63 10k
R64 10k
R66 10k
R65 10k DNP
R69 1% 12k RREF

SW1
DFU
P2_8 R30 39
R7 10k
Default boot configuration is SPIFI. Press SW1 during reset to switch to USB0 (DFU mode).
Boot selection:

	P2_9	P2_8	P1_2	P1_1
USART0	GND	GND	GND	GND
SPIFI	GND	GND	GND	VCC
USB0	GND	VCC	GND	VCC
SSP0	GND	VCC	VCC	VCC
USART3	VCC	GND	GND	GND

P73 P2_9 10k R93
P74 P1_2 10k R68
P1_1 R67 10k

SW2
RESET
R19 39
R49 10k

LED1 LED2 LED3 VCC EN1V8 VAA
R72 470 R73 1k R74 148 R75 470 R76 1k R18 148
D4 D5 D6 D7 D8 D2
VCCLED VBLED VAALED
RX TX

U23 starts up on this 12 MHz crystal. This makes it possible to use USB0 DFU boot mode. It should be possible to switch to GP_CLKIN provided by the clock generator IC (MCL_CLK) if desired.
X2
MCU_XTAL
XTAL1 XTAL2
C157 18pF
C158 18pF

C155 and C156 values are a guess. The datasheet doesn't state the acceptable voltage range for GP_CLKIN.
MCU_CLK
R34 39
P72 GP_CLKIN
C156 47pF DNP

P28
SD
SD_CD SD_DAT3
SD_DAT2 SD_DAT1
SD_DAT0 SD_VOLT0
SD_CMD SD_POW
SD_CLK
GCK2 GCK1
B1AUX14 B1AUX13
CPLD_TCK BANK2F3M2
CPLD_TDI BANK2F3M6
BANK2F3M12 BANK2F3M4

P5
LEDS
LED1 LED2
IVAA_ENABLE LED3
DNP

P0_0 P5_0 SGPIO0
P4_9 P5_1 SGPIO7
P0_1 VSSIO SGPIO9
P4_10 VDDIO SGPIO10
P1_1 SGPIO11
P1_2 SPIFI_SIO2
P1_3 SPIFI_SIO3
CLKO SPIFI_CS
P5_2 P1_4 P1_5 P1_6 P1_7 P1_8 P1_9 P1_10 P5_3 P1_11 P1_12 P5_4 P5_5 VDDREG P1_13 P1_14 P1_15 P5_6 P5_7 P1_16 P1_17 P1_18 P1_19 P9_5 P1_20 VDDIO P9_6
IVAA_ENABLE SGPIO7 LP SSP1_MISO TX_MIX_BP SSP1_MOSI SD_POW SD_CMD SD_VOLT0 SD_DAT0 SD_DAT1 RX_MIX_BP SD_DAT2 SD_DAT3 MIXER_ENX MIXER_RESETX SD_CD SGPIO10 SGPIO2 TX_AMP CS_AD SGPIO11 SGPIO12 SSP1_SCK CPLD_TDO CS_XCVR SGPIO8 SGPIO_CLK

U24
GSG-XC2C64A-7VQG100C
B2AUX12 B2AUX11 B2AUX10 B2AUX9 VAUX B2AUX8 B2AUX7 B2AUX6 B2AUX5 B2AUX4 B2AUX3 B2AUX2 B2AUX1
BANK2F1M12 BANK2F1M11 BANK2F1M10 BANK2F1M9 BANK2F1M8 BANK2F1M7 BANK2F1M6 BANK2F1M5 BANK2F1M4 BANK2F1M3 BANK2F1M2 BANK2F1M1 BANK1F2M1 BANK1F2M2 BANK1F2M3 BANK1F2M4 BANK1F2M5 BANK1F2M6 BANK1F2M7 BANK1F2M8 BANK1F2M9
DD9 DD8 DD7 GCK0 GCK1 DD6
GND NC
BANK2_AUX
B2AUX1 B2AUX3 B2AUX5 B2AUX7 B2AUX9 B2AUX11 B2AUX13 B2AUX15
B2AUX2 B2AUX4 B2AUX6 B2AUX8 B2AUX10 B2AUX12 B2AUX14 B2AUX16
P30
DNP
GCK0 GCK1
B2AUX16 BANK2F3M1 BANK2F3M2 BANK2F3M3 VCCIO2 BANK2F1M14 BANK2F1M15 BANK2F1M16 BANK2F1M1 BANK2F1M2 BANK2F1M3 VCCIO2 BANK2F3M4 BANK2F3M5 BANK2F3M6 BANK2F3M7 BANK2F3M8
CPLD_TDO
B2AUX13 B2AUX14
GND BANK2F1M13 VCCIO2 BANK2F1M14 BANK2F1M15 BANK2F1M16 BANK2F3M1 BANK2F3M2 BANK2F3M3 VCCIO2 GND TDO NC BANK2F3M4 BANK2F3M5 BANK2F3M6 BANK2F3M7 BANK2F3M8
NC BANK2F3M9 NC BANK2F3M10 BANK2F3M11 BANK2F3M12 GND BANK2F3M13 BANK2F3M14 NC NC BANK2F3M15 NC GND BANK2F3M16 BANK1F4M16 NC BANK1F4M15 VCC B1AUX14 BANK1F4M14 BANK1F4M13 NC BANK1F4M12 BANK1F4M11 VCCIO1
VCC BANK1F2M10 BANK1F2M11 BANK1F2M12 BANK1F2M13 GND BANK1F2M14 BANK1F2M15 BANK1F2M16 BANK1F4M1 BANK1F4M2 BANK1F4M3 VCCIO1 BANK1F4M4 BANK1F4M5 BANK1F4M6 BANK1F4M7 BANK1F4M8 NC TDI NC BANK1F4M9 BANK1F4M10
DD2 DD1 DD0 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0
CPLD_TDI CPLD_TCK CPLD_TMS

P29 CPLD_JTAG DNP
CPLD_TMS CPLD_TDO

R77 39 SGPIO9 BANK2F3M1
R78 39 SGPIO13 BANK2F3M2
R79 39 SGPIO0 BANK2F3M3
R80 39 SGPIO14 BANK2F3M4
R81 39 SGPIO1 BANK2F3M5
R86 39 SGPIO15 BANK2F3M6
R87 39 SGPIO7 BANK2F3M7
R88 39 SGPIO10 BANK2F3M8
R89 39 SGPIO2 BANK2F3M9
R90 39 SGPIO3 BANK2F3M10
R91 39 SGPIO11 BANK2F3M11
R96 39 SGPIO12 BANK2F3M12
R98 39 SGPIO4 BANK2F3M14
R99 39 SGPIO5 BANK2F3M15
R100 39 SGPIO6 BANK2F3M16

Series resistors are here because of a possible overshoot/undershoot problem. They may be able to be removed safely. Anyway, they probably will minimize damage in the event of SGPIO/CPLD misconfiguration.

License: GPL v2
Copyright 2012 Michael Ossmann
File: mcu.sch
Sheet: /mcu/usb/power/
Title: HackRF One mcu/usb/power
Size: User | *Date: 23 dec 2013* | Rev:
KiCad E.D.A. | Id: 4/4

C84 22pF, C85 22pF, C86 22pF, C87 10nF, C89 10nF, C90 100pF, C91 100nF, C92 10nF, C93 10nF, C94 22pF

C88 10nF

C71 100nF, C72 2.2uF, C73 100nF, C74 2.2uF, C75 100nF, C76 2.2uF, C77 100nF, C78 2.2uF, C79 100nF, C80 2.2uF, C81 100nF, C82 2.2uF, C83 100nF

C167 100nF, R11 10k, MOSFET_P Q3, VAA_ENABLE, FILTER FB2, PCB trace jumper, C105 10uF, P36 VAA DNP

test points: P37 SCL, P38 SDA, P39 SSP1_SCK, P40 SSP1_MOSI, P41 SSP1_MISO, P53 CS_XCVR, P54 CS_AD, P55 TXENABLE, P56 RXENABLE, P57 XTAL2, P58 GCK1, P59 GCK2, P60 SGPIO_CLK, P61 DA0, P62 DA7, P63 DD0, P66 DD5, P64 DD9, P67 RSSI; P83, P84, P85, P86, P87, P88, P89, P90, P91, P92

RX_IF, RX_BALUN T3, L6 DNP, C99 DNP 22pF, L7 6.2nH, C102 22pF

TX_IF, TX_BALUN T4, L8 DNP, C104 3pF, L9 DNP, C111 3pF

U17 MAX2837

0	EP		
1	VCCRXLNA		
2	GNDRXLNA		
3	B5		
4	RXRF+		
5	RXRF−		
6	B4		
7	VCCTXPAD		
8	B3		
9	B2		
10	TXRF+		
11	TXRF−		
12	B1		
13	VCCTXMX		
14	PABIAS		
15	SCLK		
16	CLOCKOUT		
17	XTAL2		
18	XTAL1		
19	VCCXTAL		
20	VCCDIG		
21	VCCCP		
22	GNDCP		
23	CPOUT+		
24	CPOUT−		
25	ENABLE	XCVR_EN	
26	GNDVCO		
27	BYPASS		
28	VCCVCO		
29	DOUT	SSP1_MISO	
30	CS	CS_XCVR	
31	DIN	SSP1_MOSI	
32	RSSI	RSSI	
33	B7		
34	B6		
35	RXBBQ−	RXBBQ−	
36	RXBBQ+	RXBBQ+	
37	RXBBI−		
38	RXBBI+		
39	VCCRXVGA		
40	RXHP		
41	VCCRXFL		
42	TXBBI−		
43	TXBBI+		
44	TXBBQ+		
45	TXBBQ−		
46	VCCRXMX		
47	TXENABLE		
48	RXENABLE		

TXBBQ−, TXBBQ+, TXBBI+, TXBBI−, RXBBI+, RXBBI−

R20 0, R21 0, R22 0, R23 0

C106 1uF, R41 10k

C95 DNP 22pF, C96 DNP 22pF

R8 1% 1k QD+, R9 1% 1k QD−, R10 1% 1k ID−, R13 1% 1k ID+

R14 1% 4k7, R15 1% 4k7, R16 1% 4k7, R17 1% 4k7

C97 330nF COM, C98 330nF REFN

C100 330nF

C101 DNP 22pF, C103 DNP 22pF, C107 DNP 22pF, C108 DNP 22pF, C109 DNP 22pF, C110 DNP 22pF

U18 MAX5864

0	EP		
1	REFP	REFP	
2	VDD		
3	IA+	IA+	
4	IA−	IA−	
5	GND		
6	CLK	GCK1	
7	GND		
8	VDD		
9	QA−	QA−	
10	QA+	QA+	
11	VDD		
12	GND		
13	DA0	DA0	
14	DA1	DA1	
15	DA2	DA2	
16	DA3	DA3	
17	OGND		
18	OVDD		
19	DA4	DA4	
20	DA5	DA5	
21	DA6	DA6	
22	DA7	DA7	
23	DD0	DD0	
24	DD1	DD1	
25	DD2	DD2	
26	DD3	DD3	
27	DD4	DD4	
28	DD5	DD5	
29	DD6	DD6	
30	DD7	DD7	
31	DD8	DD8	
32	DD9	DD9	
33	VDD		
34	SSP1_MOSI	SSP1_MOSI	
35	SSP1_SCK	SSP1_SCK	
36	CS_AD	CS_AD	
37	GND		
38	NC		
39	VDD		
40	QD+		
41	GND		
42	VDD		
43	ID−		
44	ID+		
45	REFIN		
46	COM		
47	REFN		
48	REFN		

U19 SI5351C

0	GND		
1	XA	XA	
2	XB	XB	
3	INTR	INTR	
4	SCL	SCL	
5	SDA	SDA	
6	CLKIN	CLKIN	
7	OEB	OEB	
8	CLK3	CLK3	
9	CLK2	CLK2	
10	VDDOB		
11	VDDOA		
12	CLK1	CLK1	
13	CLK0	CLK0	
14	VDDOD		
15	CLK7	CLK7	
16	CLK6	CLK6	
17	CLK5	CLK5	
18	CLK4	CLK4	
19	VDDOC		
20	VDD		

MIX_CLK, CLKOUT, CLKIN, CLK6, MCU_CLK, P14, P15 INTR, P18

R27 18, R28 18, R104 10k, X1 GSG-XTAL4PIN, C169 DNP, C170 DNP, C113 100nF

C115 33pF, C116 47pF

CLK0 is at the sample rate
CLK1 is at sample rate x2
CLK2 is at sample rate x2

R31 39 GCK1, C68 DNP 100pF

R32 39 GCK2, C69 DNP 100pF

R94 39 SGPIO_CLK, C159 DNP 100pF

R33 39 CLKOUT, C165 DNP 100pF, R105 10k

P16 CLKIN, 3.3 V CMOS clock input at 10 MHz (or 10 MHz to 100 MHz with firmware modification), D3 GSG-DIODE-1V5-BI, R85 10k

P2 CLKOUT, D9 GSG-DIODE-1V5-BI, 3.3 V CMOS clock output at 10 MHz (or other frequency with firmware modification)

C119 100nF, C120 100nF, C121 100nF, C122 100nF

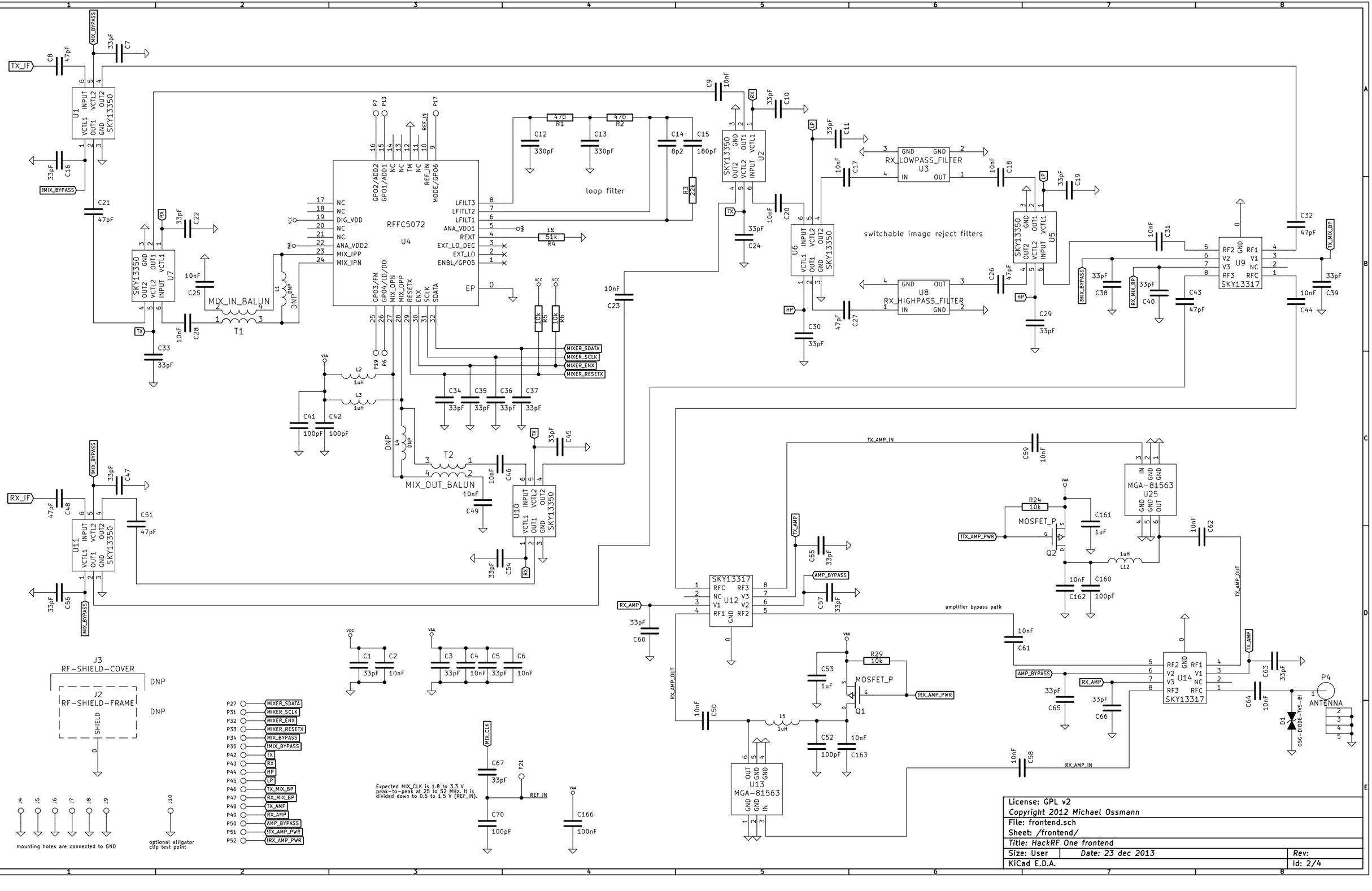
CPOUT−, C112 180pF, R25 475, R26 475, C114 3.3nF

SSP1_MISO, C168 DNP 100pF

P9 BASEBAND: RXBBI−, RXBBI+, TXBBQ+, TXBBQ−, RXBBQ−, RXBBQ+, TXBBI−, TXBBI+

C123 100nF, C124 2.2uF

License: GPL v2	
Copyright 2012 Michael Ossmann	
File: baseband.sch	
Sheet: /baseband/	
Title: HackRF One baseband	
Size: User	*Date: 23 dec 2013* — Rev:
KiCad E.D.A.	Id: 3/4


RFFC5072
U4
loop filter
MIX_IN_BALUN
T1
MIX_OUT_BALUN
T2
switchable image reject filters
RX_LOWPASS_FILTER
RX_HIGHPASS_FILTER
SKY13317
MGA-81563
MOSFET_P
ANTENNA
TX_IF
RX_IF
MIX_BYPASS
!MIX_BYPASS
TX_AMP_IN
RX_AMP_OUT
amplifier bypass path
Expected MIX_CLK is 1.8 to 3.3 V peak-to-peak at 25 to 52 MHz. It is divided down to 0.5 to 1.5 V (REF_IN).
mounting holes are connected to GND
optional alligator clip test point
License: GPL v2
Copyright 2012 Michael Ossmann
File: frontend.sch
Sheet: /frontend/
Title: HackRF One frontend
Size: User
Date: 23 dec 2013
Rev:
KiCad E.D.A.
Id: 2/4